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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/796,484	03/08/2004	Daniel Lee Avery	US 030078	2303

24738 7590 09/26/2006

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EXAMINER	
TU, CHRISTINE TRINH LE	

ART UNIT	PAPER NUMBER
2138	

DATE MAILED: 09/26/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/796,484	AVERY ET AL.	
	Examiner	Art Unit	
	Christine T. Tu	2138	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 June 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5, 9, 12-13, 15, 17-21 and 23-25* is/are rejected.

7)☒ Claim(s) *6-8,10,11,14,16 and 22* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 June 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

1. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Double Patenting

2. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

3. Claims 19, 21 and 22 are again provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 23, 26 and 27 of copending Application No. 10/796,480, respectively. Although the conflicting claims are not identical, they are not patentably distinct from each other because the copending application '480 teaches the claimed invention. The copending application '480 does not explicitly teach the configurator server. The copending application '480, however, teaches the "configurator circuit" (at line 5 of claim 23). It would have been obvious to one skilled in the art at the time the invention was made to

realize that the configurator circuit (as taught by the copending application '480) would have been named as "configurator server". One having ordinary skill in the art would be motivated to do so because naming the configurator circuit (of the copending application '480) as "configurator server" would not affect the functionality of the configurator circuit.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Claim Rejections - 35 USC § 103

4. Claims 1-5, 9, 12-13, 15, 17-21 and 23-25 are again rejected under 35 U.S.C. 103(a) as being unpatentable over Garreau (6,425,101).

Claims 1, 3:

Garreau discloses the invention substantially as claimed. Garreau discloses (figures 2 & 4 & 7) a test network (200) including a master controller (202) connected to a programmable switch (204 or 408). The programmable switch (204) is connected to a slave target device (206) containing JTAG compliant integrated circuits (IC1 through IC4). The master controller (20) further comprises a JTAG controller (210) and a switch controller (218) for providing JTAG test protocols by using an I/O line (211-1) and data to the slave target device (206), and receiving the test results by using the feed backward line (211-2) via the programmable switch (204 or 408) (figures 2 & 4, column 4 lines 41-column 5 line 36).

Garreau does not explicitly teach the controllable switches. Garreau, however, teaches (figure 4) that the programmable switch (208) comprises a plurality of vertical data lines (402) and programmably connected to horizontal data lines (404) forming a "crossbar" switch. Each of the horizontal data lines (404) is connected to one of the programmable switch I/O lines (410). Each of the programmable switch I/O switch I/O lines (410) are in turn connected in a pair-wise manner to the ICs (IC1 through IC4) located on the target hardware device (206) such teach each IC can be selectively tested (column 6 lines 49-column 7 lines 28).

It would have been obvious to one skilled in the art at the time the invention was made to realize that Garreau's combination of plurality of vertical data lines (402) and the plurality of the horizontal data lines (404) (in Garreau's programmable switch [208]) would have been the controllable switches. One having ordinary skill the in the art would be motivated to realize so because Garreau's combination of vertical data lines (420) and horizontal data lines (404) are used for selectively connecting a IC [in the target device (206)] to the master controller (202) (column 7 lines 12-28).

Claim 2:

Garreau further teaches (figure 4) that the programmable switch (400) further comprises a connector (412-10) to connect a vertical data line (402-3) to the JTAG controller (210) by way of the I/O line (211-2) wherein the I/O line (211-2) feeds back the test results. The programmable switch (400) also comprises a connector (412-9) to connect the vertical data line (402)-4 to the JTAG controller (210) by way of the I/O line (211-2) (figure 4, column 8 lines 48-58; column 5 lines 10-36).

Claim 4:

Garreau further teaches (figure 4) that the programmable switch (400) further comprises a connector (412-10) to connect a vertical data line (402-3) to the JTAG controller (210) by way of the I/O line (211-2) wherein the I/O line (211-2) feeds back the test results. The programmable switch (400) also comprises a connector (412-9) to connect the vertical data line (402)-4 to the JTAG controller (210) by way of the I/O line (211-2). In this way the integrated circuits IC3 and IC2 can be tested and are daisy-chained in the JTAG path in responsive to the appropriate switch control signal from the switch controller (218) (figure 4, column 7 lines 29-58; column 5 lines 10-36).

Claim 5:

Garreau teaches (figure 7) a host computer (72) provides a user interface for sending corresponding configuration data to the master controller (704) then directs the programmable witch (706) to connect which of ICs (708 through 714) to be tested (figure 7, column 8 lines 57-column 9 line 5).

Claim 9:

Garreau teaches (figure 7) a host computer (72) provides a user interface for sending corresponding configuration data to the master controller (704) then directs the programmable witch (706) to connect which of ICs (708 through 714) to be tested (figure 7, column 8 lines 57-column 9 line 5).

Garreau does not explicitly teach a memory for storing the corresponding configuration data before sending such configuration data to the master controller (704).

However, it would have been obvious to one skilled in the art at the time the invention was made to realize Garreau's host computer (702) would have comprised a memory for storing such configuration data. One having ordinary skill in the art would be motivated to realize so because having a memory for storing (configuration) data inside a computer (or a host computer) is well-known in the art.

Claims 12, 15 and 24-25:

Claims (12, 24, 25) and 15 are rejection for reasons similar to those set forth against claims (1 & 5) and 4, respectively.

Claim 13:

Garreau also teach that the horizontal data line controller (408) and the vertical data line controller (408), in responsive to the control signals, uses the connector (412-9) to connect the vertical data lines (402-4) by the way of the I/O line (211-1), and use the programmable connector (412-10) to connect the vertical data line (402-3) by way of the I/O line (211-1) (figure 5 lines (column 7 lines 37-54).

Claims 17 & 18:

Garreau's master controller (704) directs the programmable switch (706) to selectively couple an IC in responsive to the configuration data from the host computer (702) (figure 7, column 8 lines 62-622).

Claim 19:

Claim 19 is rejection for reasons similar to those set forth against claims (1 & 5) except that a memory with program software is recited. However, Garreau teaches (figure 7) that the host computer (702) provides executable instructions to a test network (703) (figure 7, column 8 lines 50-52).

Claims 20-21 & 23:

Claims (20 & 23) and 21 are rejection for reasons similar to those set forth against claims 15 and (17 & 18), respectively.

Response to Arguments

5. Applicant's arguments filed June 28, 2006 have been fully considered but they are not persuasive.

For provisionally obvious-type double patenting rejections of claims 1-6, 9, 12-15, 17, 19, 21-22 and 24-25, applicant argues that the rejection fails to provide any rationale behind the rejection. Examiner has been withdrawn the provisionally obvious-type double patenting rejections of many claims except for claims19 and 21-22.

For claims 19, 21 and 22, these claims are so similar to claims 23, 26 and 27 of the copending application '480, respectively. Especially, claim 23 of the copending application '480 is recited with all elements in claim 19 of this application '484 except the different name-usage of the term "configurator **circuit**" in application '480 and the term "configurator **server**" in application '484 (see rejection in ¶3 above). Therefore claims 19, 21 and 22 are still rejected under provisionally obvious-type double patenting.

For the section 103(a) rejections in claims 1, 12, 14 and 25, the applicant argues that Garreau reference does not teach a communications link adapted to communicatively couple an external user-controlled device and a programmable microcontroller for passing reconfiguration-control signals to the programmable microcontroller. Examiner, however, disagrees against applicant's remark. Garreau does teach such limitations. Garreau teaches a link between the host computer (702) [having a user interface] and the master controller (704). Such a link for providing necessary configuration data to the master controller (704) to provides instructions to the master controller (704) (figure 7, column 8 lines 57-58, column 8 line 62-column 9 line 11).

For claim 19, Applicant alleges that Garreau reference does not teach the limitations of routing JTAG test signals along a JTAG circuit path on at least one of the inter-connectable circuit boards (e.g. via a reprogrammable microcontroller—as in figure 4).

Examiner, however, respectfully traverses applicant's position. Firstly, applicant should aware that patentable weight is limitation to the claimed language only. So such a drawing (figure 4) or an example (e.g. via a reprogrammable) does not play a role of any patentable weight at this point.

Secondly, at lines 8-11 of claim 19, the claim is actually recited with "... the ...routing switches in response to a signal detected from at least one of the JTAG test modes for routing JTAG test signals along a JTAG circuit path on at least the first one of

the inter-connectable circuit boards". In other words, what is being claimed is that the routing switches are actually performing the routing, not the microcontroller.

Garreau does teach such routing limitations. Garreau teaches that under the control of the JTAG controller (210) and the switch controller (218), the programmable switch (204) to feed/route test protocol to the IC (IC1) via (220) on a slave target device (206) (figure 2, column 5 lines 26-36).

For claims 4, 15, 20 and 23, applicant further alleges that Garreau does not teach the limitations of JTAG signal path switches adapted to route JTAG signals on a configured circuit or between a configured circuit and other configured circuit coupled to the configured circuit. Garreau does teach such limitation. Garreau teaches that the integrated circuits IC3 and IC2 can be connected in a daisy chain in the JTAG path and tested in responsive to the control from the master controller (202) (figure 4, column 7 lines 29-58).

6. Claims 6-8, 14, 16 and 22 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christine T. Tu whose telephone number is (571)272-3831. The examiner can normally be reached on Mon-Thur. 8:30am-6:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on (571)272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Christine T. Tu
Primary Examiner
Art Unit 2138

September 17, 2006